Storage IP for Automotive Applications, a Bottleneck Relief

Cadence Design Systems

ABSTRACT

Self-driving cars seem to be the next big thing in automotive. There is no doubt that in order to accomplish this complicated technological feat, one would have to acquire a huge amount of information from multiple cameras, RADARs, LiDARs, and proximity sensors. Processors and DSPs handle the huge amounts of data being streamed in, and doing so in real time. “So, where is the bottleneck in the system?” you may ask. Processing power scales very nicely, but storing this information to non-volatile automotive-grade memory is not as trivial as one may think. This information is stored for legal reasons, to be able to analyze the system’s behavior and decision making in case an accident occurs. This raw information is also very useful for debugging the system and improving it by implementing machine learning algorithms. In this presentation, we will review the various existing non-volatile storage solutions, and focus on serial flash variants that provide both the bandwidth and capacity needed, as well as the reliability and ease of use. We will do a deep dive on flash memory sub-systems including performance tradeoffs and the type of interface IPs needed to support such sub-systems. In particular, address the key active safety features that are needed to meet the ASIL-readiness criteria for functional safety.

Storage IP for Automotive Applications, a Bottleneck Relief

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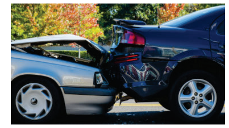
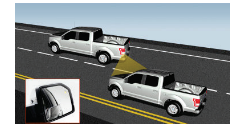
Automotive Safety and ADAS Evolution



Collision Warning/Avoidance

Pedestrian Detection Warning

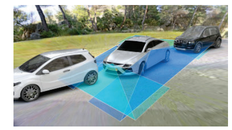


Blind Spot Monitor

Autonomous Self Driving

www.tesla.com

Night Vision



Surround View Camera

Parking Asist

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Diversity and Complexity of ADAS Applications

Demands high-performance and flexible compute and storage platform

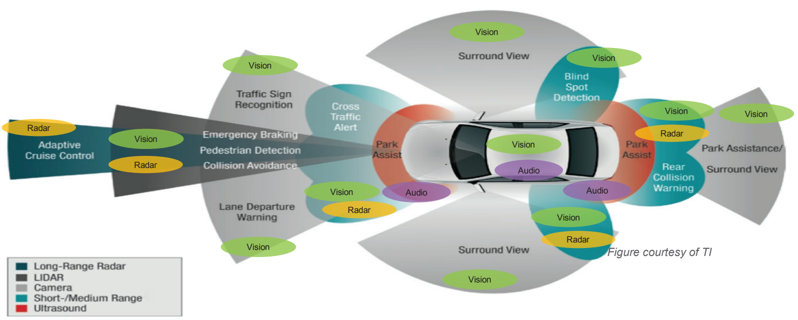

Figure courtesy of TI

Vision		Radar	Audio/Sound
Rear-View Camera Vision Enhancement Auto-Dimming Headlights Blind-Spot Detection 360 View Parking Assist Sign Recognition Traffic Signal Detection	Lane Detection Rain/Fog Detection Pedestrian Detection Pedestrian Avoidance Eye Focus Detection Driver Monitoring Sign Recognition Vehicle Detection	Front Collision Avoidance Braking Adaptive Cruise Control 360-Degree Hazard Awareness Rear Collision Detection	Rear Object Detection Parking Assist/Auto Park Voice Recognition Cabin Noise Reduction Emergency Recognition

Vision and radar data must be stored for legal and other reasons

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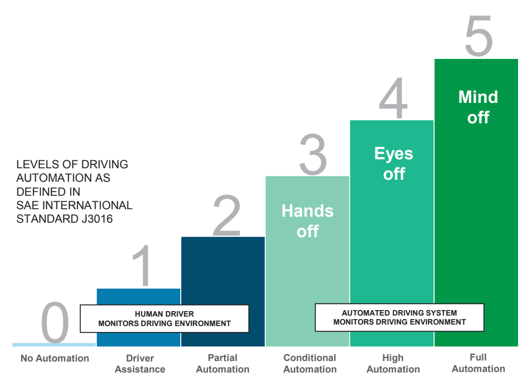
Autonomous Driving

"With great power comes great responsibility"

- Amount of electronics is growing fast (with the level of automation)
- Number of sensors and cameras increases for every level of automation
- Image quality (resolution, frame per second) requirements increase for higher levels of automation
- Advanced driver assistance systems (ADAS) are based on complex SoCs
- Result is more data to stream, process, and store!



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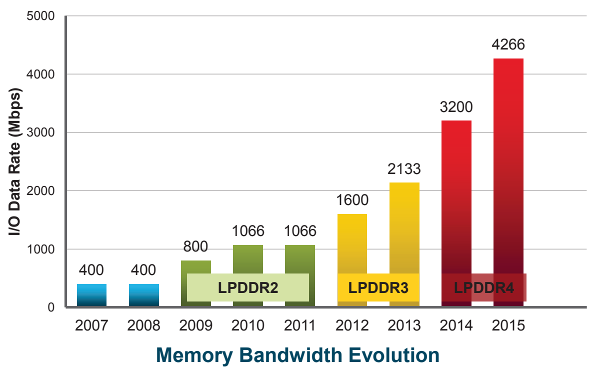
Increased Storage/Memory Bandwidth Demand



- # of Cameras
- Camera Resolution
- Frame Rate
- # of Streams / Camera
- Data to Be Stored

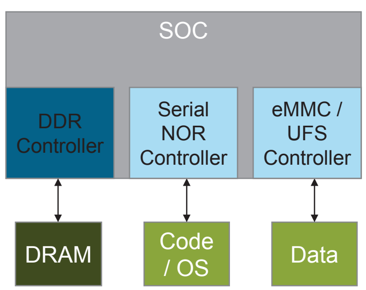
ADAS introduces more cameras, better image quality → more data to move and store
Automotive DRAM evolves to handle it—and so should non-volatile memory!

Comparing Storage and Memory Types

	DRAM	Parallel NOR	Quad / Octal SPI	eMMC	UFS
Nonvolatile	No	Yes	Yes	Yes	Yes
Read/Write Resolution	Byte	Byte	Byte	Page	Page
Write Speed	VVVVV	V	V	VVV	VVVV
Read Speed	VVVVV	VV	VVV	VVV	VVVV
XIP	Yes	Yes	Yes	No	No
Density	High	Low	Low	Highest	Highest
$ per bit	$$	$$$	$$$	$	$
Application	Main Memory	Code / Firmware	Code / Firmware	Data	Data

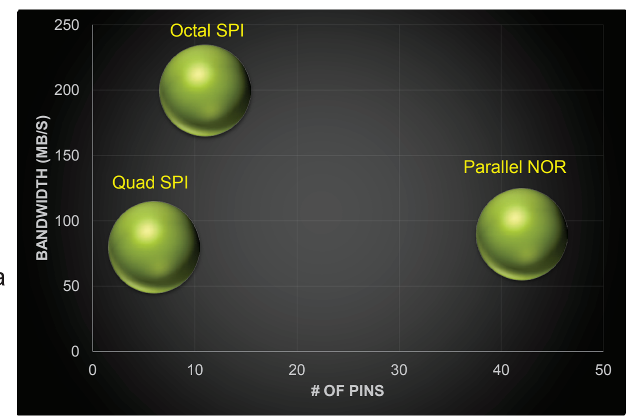
Storage Architecture in Typical Automotive SoC

- Code storage utilizing serial NOR flash
  - Quad / Octal SPI
  - Up to 400MB/s bandwidth
  - Store boot code and OS + "apps"
  - XIP (eXecute In Place) support
- Data storage utilizing eMMC or UFS
  - Bandwidth over 1GB/s
  - Faster writes (100s of MB/s)
  - Higher density (256GB devices available)
  - Store vision and other "black box" data
  - Cheaper $/GB



Code Storage – Available Options

- ✓ Octal SPI delivers more than 2X bandwidth at ¼ pins
- ✓ Package size much smaller → smaller PCB
- ➢ Octal SPI requires a controller (Parallel NOR does not)

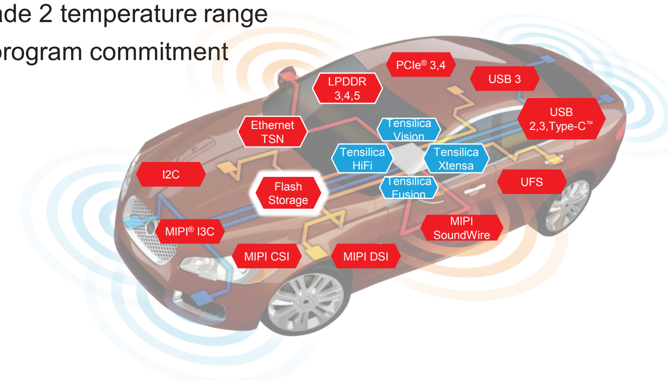


Lower pin count for improved reliability and simpler design while improving performance!

Cadence IP Automotive Solution

Major focus on automotive with ASIL-B-ready IP

- ISO 26262-certified R&D centers in:
  - UK, Poland, India, China, US, Canada
- FMEDA audited for ASIL-B readiness
- AEC-Q100 grade 2 temperature range
- TSMC9000A program commitment



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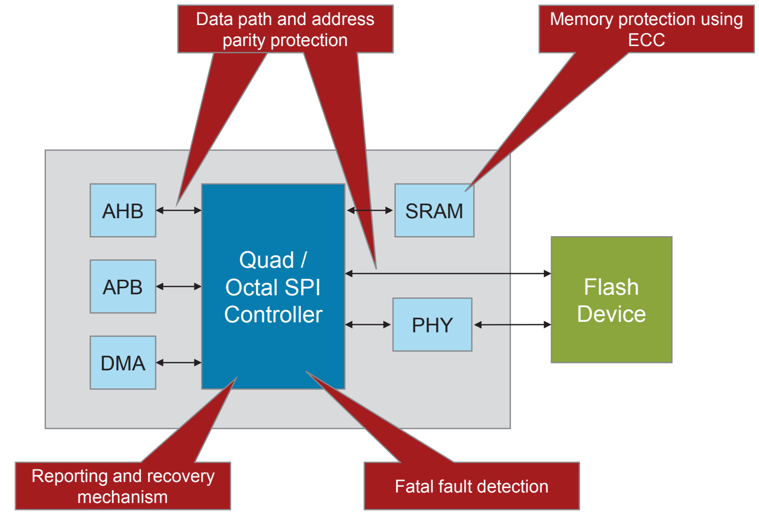
Active Safety Features



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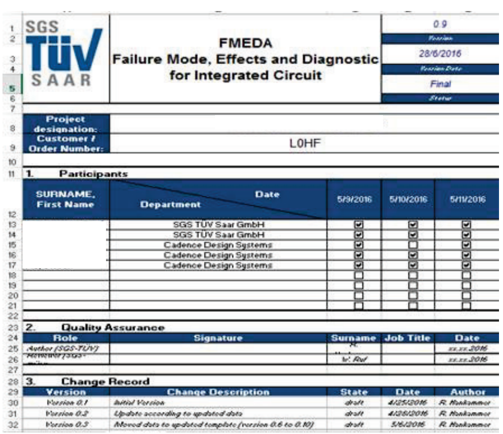
Automotive-Specific Deliverables

- FMEDA report
- Safety manual
- ISO 26262 ASIL readiness certificate


SGS TÜV SAAR

FMEDA
Failure Mode, Effects and Diagnostic for Integrated Circuit

0.9 — Version
28/6/2016 — Version Date
Final — Status

Project designation:
Customer / Order Number: L0HF

1. Participants

SURNAME, First Name	Department / Date	5/9/2016	5/10/2016	5/11/2016
	SGS TÜV Saar GmbH	☑	☑	☑
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	Cadence Design Systems	☑	☐	☑
	Cadence Design Systems	☑	☑	☑
	Cadence Design Systems	☑	☑	☑

2. Quality Assurance

Role	Signature	Surname	Job Title	Date
Author (SGS-TÜV)				xx.xx.2016
Reviewer (SGS-...)				xx.xx.2016

3. Change Record

Version	Change Description	State	Date	Author
Version 0.1	Initial Version	draft	4/25/2016	R. Hankammer
Version 0.2	Update according to updated data	draft	4/26/2016	R. Hankammer
Version 0.3	Moved data to updated template (version 0.6 to 0.10)	draft	5/6/2016	R. Hankammer

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In Summary

- ADAS and autonomous driving introduces A LOT more sensory data
- DSP and DRAM already dealing with additional processing and bandwidth required by the increase in data
- Nonvolatile memory needs to catch up, too
- Parallel NOR is not fast enough for bigger OS and application images (too long to "boot up")
- Quad and Octal SPI memories—the answer for faster code and firmware storage
- UFS and eMMC for fast and reliable mass storage

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